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Mission Profile Translation to Capacitor Stresses in Grid-Connected Photovoltaic Systems

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***Abstract*— DC capacitors are widely adopted in grid-connected PhotoVoltaic(PV) systems for power stabilization and control decoupling. They have become one of the critical components in grid-connected PV inverters in terms of cost, reliability and volume. The electrical and thermal stresses of the DC capacitors are varying along with the intermittent solar PV energy (i.e. of weather-dependency) and also the grid conditions (e.g. voltage fault transients). This paper serves to translate real-field mission profiles (i.e. solar irradiance and ambient temperature) into voltage, current, and temperature stresses of the DC capacitors under both normal and abnormal grid conditions. As a consequence, this investigation provides new insights into the sizing and reliability prediction of those capacitors with respect to prior-art studies. Two study cases on a single-stage PV inverter and a two-stage PV inverter are demonstrated by simulations and experiments. The results have verified the discussions.**

I. Introduction

Grid-connected PhotoVoltaic (PV) systems have experienced spectacular periods of increasing installations in recent years, and the penetration level of PV systems will be further enhanced in near future [1]. In order to reduce the cost of energy by means of increasing efficiency and extending lifetime, advanced control strategies have been developed for a vast amount of grid-connected topologies [2]–[8]. However, even with those advanced control methods and dedicated Maximum Power Point Tracking (MPPT) algorithms, the power extracted from the PV panels is time varying and dependent on mission profiles (e.g. ambient temperature and solar irradiance level), which contributes to a mismatch between the Direct-Current (DC) power extracted from PV panels and the instantaneous Alternative-Current (AC) power fed into the grid. Therefore, the power difference has to be balanced using energy storage elements in those PV systems. Conventionally, capacitors are widely used at the DC-link and serve as the energy storage elements to perform functions like power balancing, ripple-voltage limiting, and sufficient energy provision during the hold-up time of the system [9]–[11].

Regarding the design of the DC-link capacitors in PV systems, it embraces many considerations, e.g. voltage rating, ripple current rating, efficiency, volume, cost, stability, and etc.. For example, a severe voltage overshoot on the DC-link, which will induce failures to the capacitor and thus the system, has been witnessed in a fuel cell system during fault ride-through [12]. Hence, many efforts have been made to enhance the performance of DC-link capacitors by means of reducing the stresses and the capacitance without loss of performance. In [13] and [14], the capacitor stress in adjustable-speed drives under abnormal input conditions has been discussed, in which it has been revealed that the operation conditions would make a contribution to the capacitor lifetime. Additionally, in [15] is introduced a reliability-oriented design approach for capacitors in PV applications considering the operation conditions. Besides, in [16] and [17], solutions to reduce the capacitance have been proposed. It has also been found that the reduction of capacitance can contribute to high power density and allow cost-effective solutions with advanced capacitor technologies of high reliability, e.g. film capacitors, to be used in PV systems. Use of the above solutions can achieve more reliable operations of DC capacitors in the normal operation mode (e.g. MPPT). However, minimum energy and capacitance requirements have to be fulfilled; otherwise, the system may run into instability during operation [18].

In addition to the above solutions, possibilities to reduce the capacitance are based on the following approaches: a) ripple current reduction with sophisticated control, b) cancellation circuit with coupled elements, c) voltage ripple reduction by increasing its frequency, and d) active power filters, which adopt auxiliary circuits in parallel with DC-link capacitors. In [10], a benchmarking of various power decoupling techniques for PV micro-inverters with different DC-link capacitor locations has been provided in terms of cost, efficiency, and control complexity. However, all those solutions to reduce the size of the required capacitance of the DC-link capacitors, and thus improvement of capacitor reliability, are mostly discussed under normal operation modes with constant environmental conditions. To our knowledge, there are few studies concerning the effect on DC-link capacitors from mission profiles, while mission profile based research is of intense interest for the power electronics converters [11], [15], [19], [20].

In view of the above issues, a mission profile translation to capacitor stresses in single-phase grid-connected PV systems

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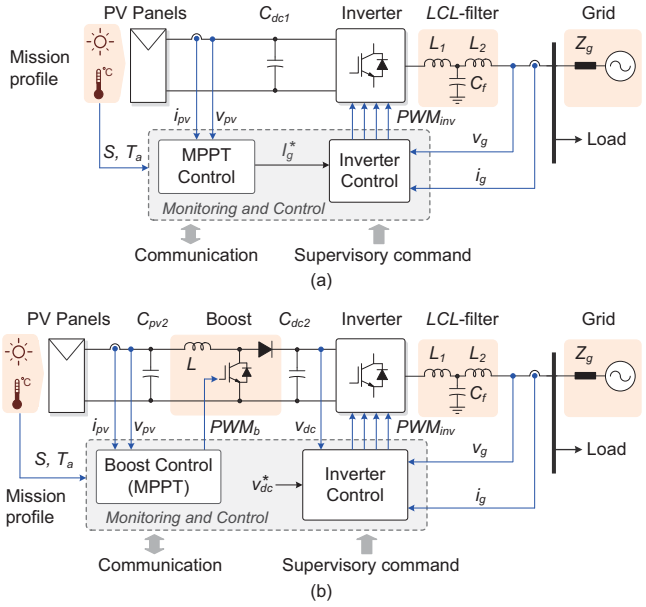

Fig. 1. Typical configurations and overall control structures of single-phase grid-connected PV systems with low power ratings for residential applications, where capacitors are used as the energy storage elements: (a) single-stage configuration and (b) double-stage configuration.

TABLE I

PARAMETERS OF THE SINGLE-PHASE PV SYSTEMS SHOWN IN FIG. 1.

Parameter	Value
Boost converter inductor	$L = 5$ mH
LCL-filter	$L_1 = 2$ mH $L_2 = 3$ mH $C_f = 4.7$ μF
Damping resistor of *LCL*-filter	$R_d = 10$ Ω
Switching frequencies	$f_b = f_{inv} = 10$ kHz
Sampling frequency	$f_s = 10$ kHz
MPPT sampling frequency	$f_{mpp} = 200$ Hz
Grid nominal voltage (RMS)	$v_{g,RMS} = 230$ V
Grid nominal frequency	$\omega_0 = 2\pi \times 50$ rad/s

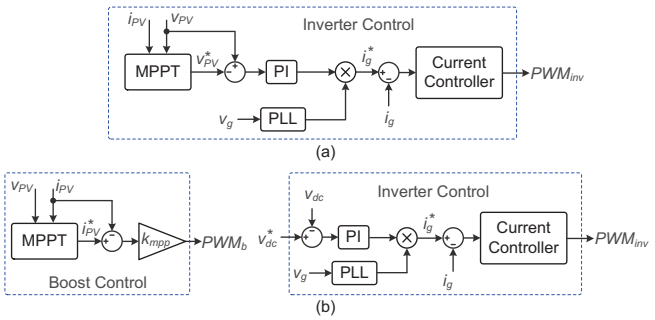

Fig. 2. Control diagram of single-phase grid-connected PV systems: (a) single-stage configuration and (b) double-stage configuration.

is in focus in this paper. The effect of the operating conditions, e.g. grid faults, on the capacitors has also been explored in § IV. Firstly, the basic stress analysis of the capacitors in single-stage and double-stage grid-connected PV systems is provided in § II considering both electrical and thermal models of the capacitor. Focused investigations of mission profile effects on capacitors are demonstrated by a 3 kW single-phase PV systems considering a real-field daily mission profile in § III. Finally, a 1 kW single-phase single-stage PV system has been tested in low voltage ride-through operation mode to reveal its effects on the capacitors (e.g. voltage stress, current stress and temperature stress) under grid faults. Both investigations contribute to new insights into the sizing and reliability prediction of the capacitors.

II. CAPACITOR DESIGN, MODELS AND STRESS ANALYSIS

A. System Description and Control

The PV systems considered in this paper are for residential applications with the nominal power of 1 kW to 3 kW. As it is shown in Fig. 1, a single-phase connection of such PV systems is commonly adopted, which can be configured as single-stage or double-stage. Currently, the PV systems of such a power rating should operate at unity power factor with an MPPT control [2]. The inverter can be transformerless in order to increase the overall efficiency. In this paper, a full-bridge topology with a bipolar modulation scheme has been used as the DC-AC conversion stage considering the elimination of leakage currents. In addition, the injected current quality is enhanced by an *LCL*-filter between the inverter and the power grid. The system parameters are given in Table I.

For the single-stage configuration, the control system applied to the inverter has to accomplish both MPPT and current shaping tasks, as it is illustrated in Fig. 2(a). In this case, the decoupling capacitor, C_{dc1}, can only be placed at the terminals of PV panels as shown in Fig. 1(a). The MPPT output (v_{pv}^*) is controlled through a Proportional Integrator (PI) controller, which produces the current amplitude reference (I_g^*) for the current controller. As for the double-stage configuration, a boost converter can be adopted and it also offers much controllability, e.g. MPPT, advanced active power control [4] and extended operational time. There are two capacitors in this system, as it is shown in Fig. 1(b). The control system can also be divided into two parts - boost control and inverter control as shown in Fig. 2(b). In the boost control system, a proportional controller (k_{mpp}) can be used to force the PV current to follow the MPPT output. The DC-link voltage (v_{dc}) is controlled through a PI controller to guarantee the power injection into the grid.

In both configurations, a Phase Locked Loop (PLL) should be utilized in order to achieve unity power factor operations as required by standards. Regarding the current controller, a Proportional Resonant (PR) controller in the $\alpha\beta$-reference frame enables a good grid current tracking compared to a PI controller, which requires current decoupling in the dq-reference frame. In order to further strengthen the power quality of the injected grid current in terms of lower total harmonic distortions, resonant or repetitive based harmonic compensators should be incorporated into the control system in parallel with the fundamental current controller [4].

B. Capacitor Sizing

In accordance to Fig. 1, on the assumption that the grid injected current i_g and the grid voltage v_g are pure sinusoidal, i.e. $i_g = I_g \cos(\omega_0 t)$ and $v_g = V_g \cos(\omega_0 t)$ with ω_0 being the fundamental grid frequency and I_g, V_g being the amplitudes of the grid current and voltage respectively, the instantaneous power $p_o(t)$ can be given as: $p_o(t) = \frac{1}{2}V_g I_g + \frac{1}{2}V_g I_g \cos(2\omega_0 t)$ in unity power factor operation. It can be seen that $p_o(t)$ consists of fluctuating power at twice the fundamental frequency, which has to be decoupled using the capacitor since the PV output power is normally controlled as constant (with high frequency pulsation) [3], [10], [15]. Hence, the electrical stresses of the inverter input capacitor (C_{dc1} or C_{dc2}) can simply be calculated as,

$$\Delta v_{dc} \approx \frac{P_o}{2\pi f_0 C_{dc} V_{dc}} \tag{1}$$

$$i_{c,RMS} = \frac{P_o}{\sqrt{2} V_{dc}} \tag{2}$$

where $P_o = \frac{1}{2}V_g I_g$ is the average power supplied to the grid, $f_0 = \omega_0/(2\pi)$ is the fundamental frequency of the grid, Δv_{dc} is the peak-to-peak ripple of the capacitor voltage V_{dc}, and $i_{c,RMS}$ is the Root-Mean-Square (RMS) current flowing through the DC capacitor.

Eq. (1) can be adopted for the DC-link (inverter-side) capacitor sizing in both single-stage and double-stage configurations. In this paper, for example, the DC-link voltage of C_{dc1} or C_{dc2} is controlled as $v_{dc}^* = 400 \pm 10$ V in both systems for comparisons, which will lead to a 5 % voltage ripple across the capacitor ($\Delta v_{dc} = 20$ V). In the case of the power rating of 3 kW, the required capacitance is: $C_{dc1} = C_{dc2} = 1200$ μF, while in this paper, it has been selected as 1100 μF with the corresponding $\Delta v_{dc} = 21.7$ V.

In respect to the sizing for the PV side capacitor C_{pv2} in a double-stage system, it is mainly dependent on the MPPT control algorithm (perturbing step-size) and also the power level, as it is shown in Fig. 3, where the capacitance of C_{pv2} is 2200 μF. It can be seen that a small perturbing step-size can contribute to a small voltage ripple and thus less power losses , but a slow transient [21]. In that case, a capacitor of smaller value can be adopted as the PV-side capacitor in a double-stage system [22]. However, as it is shown in Fig. 3(b), the voltage ripple is also affected by the solar irradiance level (the power level). Hence, considering a low PV voltage level depending on the mission profiles (e.g. weak solar irradiance and/or high ambient temperature) and the need for almost ripple-free voltage, a capacitor of larger value (C_{pv2} = 2200 μF) is selected in the case of a double-stage topology with ΔI = 0.1 A in this paper, which will approximately contribute to a 1.8 % voltage ripple ($\Delta v_{pv} = 4.7$ V) at the PV-side capacitor. The parameters of these capacitors are given in Table II.

It should be pointed out that the above capacitor sizing only takes the basic criteria and the steady state into account (i.e. voltage stresses). However, an inappropriate capacitor design may challenge the stability of the control system and the reliability of the entire power conversion system [23]. Consequently, optimization of the DC capacitor in single-phase PV systems considering transient performance and stability could be an extensive study, which is beyond the focus of this paper (i.e. it is focused on mission profile translation).

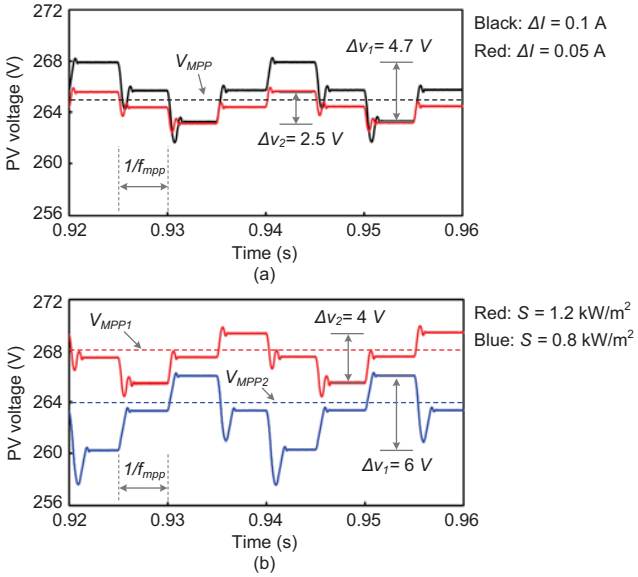

Fig. 3. Voltage stresses of the PV-side capacitor C_{PV2} in a double-stage 3 kW system using perturb and observe MPPT control algorithm (ambient temperature: 25 °C): (a) different current perturbing step-size ΔI (solar irradiance level S = 1 kW/m^2) and (b) different solar irradiance level S (current perturbing step-size ΔI = 0.1 A).

TABLE II

PARAMETERS OF THE SELECTED CAPACITORS.

Parameter	Value
Ratings	2200 μF, 385 V
ESR at 20 °C	38 mΩ at 100 Hz 20 mΩ at 100 kHz
Thermal resistance	R_{th} = 2.3 °C/W

Notes: Two caps in series for C_{dc1} and C_{dc2}.

C. Capacitor Thermal Modeling and Lifetime

An electrolytic capacitor can be modeled as an ideal capacitor in series with an Equivalent Series Resistor (ESR) and an Equivalent Series Inductor (ESL), as it is shown in Fig. 4. Due to the capacitor ESR, which is frequency-dependent [13], the double-line frequency components at the DC-link (C_{dc1} or C_{dc2}) and also the mission profile effect (MPPT control) at the PV side capacitor (C_{dc1} or C_{pv2}) will contribute to the capacitor power losses, as they are fluctuating and contain high frequency components [14], [15]. Consequently, the internal of the capacitor may be heated up due to the power loss dissipation as shown in Fig. 4, which further elaborates the relationship between capacitor power losses and the hot-spot temperature. Notably, the internal hot-spot temperature is the main failure mechanism of the capacitor [14], [15].

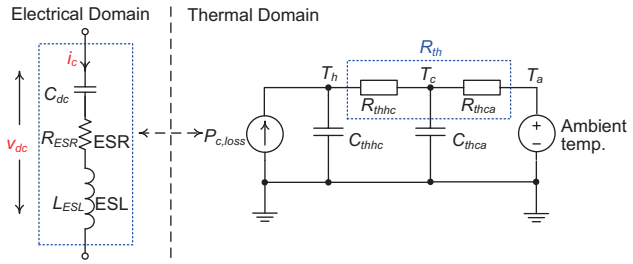

Fig. 4. Coupled relationship between the electrical and thermal models of electrolytic capacitors.

Due to the coupled relationship between the electrical and thermal performance of capacitors, the power losses have to be calculated at articular frequencies in order to estimate the lifetime of the capacitor considering short-term or long-term mission profiles. This can be enabled by the Fast Fourier Transform (FFT) of the ripple current of the capacitor [13], [14]. Thus, the total power losses can be given as,

$$P_{c,loss} = \sum_{h=1}^{N} I_{ch}^2 \cdot ESR(f_h) \tag{3}$$

where N is the number of the time-series points of the capacitor ripple current, I_{ch} is the harmonic amplitude of the capacitor current, and $ESR(f_h)$ is the corresponding ESR at the harmonic frequency, f_h, which can be found in the data-sheet of the capacitor. According to Fig. 4, the steady-state hot-spot temperature of a capacitor can be calculated as,

$$T_h = P_{c,loss} R_{th} + T_a \tag{4}$$

in which T_h is the hot-spot temperature, T_a is the ambient temperature, and R_{th} is the thermal resistance of the capacitor provided in the data-sheet. With the resultant hot-spot temperature T_h, the capacitor operating hours (lifetime) can then be estimated [13], [15].

D. Stress Analysis and Mission Profile Translation

It can be seen in (1) and (2) that the capacitor (C_{dc2}) of larger value will contribute to smaller voltage variations Δv_{dc} (ripples) in a double-stage system [13]–[15]. However, a trade-off between ripple-voltage and thermal stress has to be made during the design phase of a PV inverter system. This is almost the same case for the capacitor C_{dc1} in a single-stage system, as it is also directly connected to the PV inverter, which will produce current ripples and also voltage ripples of a twice grid fundamental frequency.

On the other hand, according to Fig. 1, the capacitor C_{dc1} has also to decouple the fluctuated power from the PV panels, which is affected mainly by ambient conditions (i.e. mission profiles) and also the MPPT control algorithm. Thus, the decoupling capacitor C_{dc1} in a single-stage system is required to withstand both a varying DC-link voltage (i.e. v_{mpp}) and maintain a smooth power at the same time. It implies that the C_{dc1} of larger value is preferable for single-stage PV systems as also discussed above. In respect to the PV-side

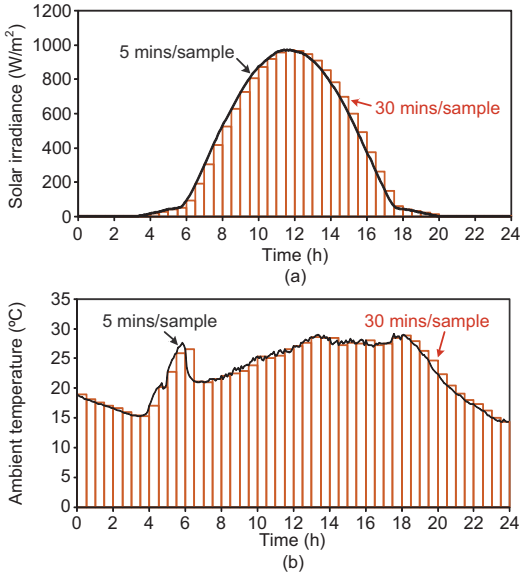

Fig. 5. A real-field daily mission profile (solar irradiance and ambient temperature, 2 samples per hour) used in the simulations.

capacitor, C_{pv2}, in a double-stage system, it only has to deal with the extracted power from the PV panels, which means that the stresses of the capacitor, C_{pv2}, is dependent on mission profiles. Hence, in same cases (e.g. a cloudy day), the PV-side capacitor, C_{pv2}, might experience larger ripples compared to the inverter capacitor (C_{dc2}) in a double-stage system. In a summary, it can be predicted that the capacitors at the PV-side (C_{dc1} and C_{pv2}) are under more ambient-dependent stresses or ripples compared to the capacitor C_{dc2} at the inverter side in a double-stage system, and the mission profiles have major contributions of those stresses of the PV-side capacitors.

Although the FFT is an effective way to analyze the harmonic components of the capacitor ripple current and then calculate the total power losses, there is still an open issue to estimate the lifetime online and under a long-term mission profile, which has been applied to lifetime estimation of semiconductors. In addition, the existing thermal models of capacitors have to be further enhanced in order to reflect the high frequency ripple current effects on the capacitor lifetime, which requires in-depth theoretical analysis. With this consideration, in the following, long-term mission profiles will be translated to the electrical stresses, including ripple current and voltage variations on the capacitor, and also the thermal loading of the capacitor, where only considering a limited number of the harmonics of the capacitor ripple currents.

III. Long-Term Mission Profile Translation to Capacitor Stresses

In order to verify the above analysis of mission profile effects on the capacitors, referring to Fig. 1, a real-field daily mission profile as shown in Fig. 5 has been used, and it has been translated to the voltage and current stresses of the capacitors in both single-stage and double-stage single-

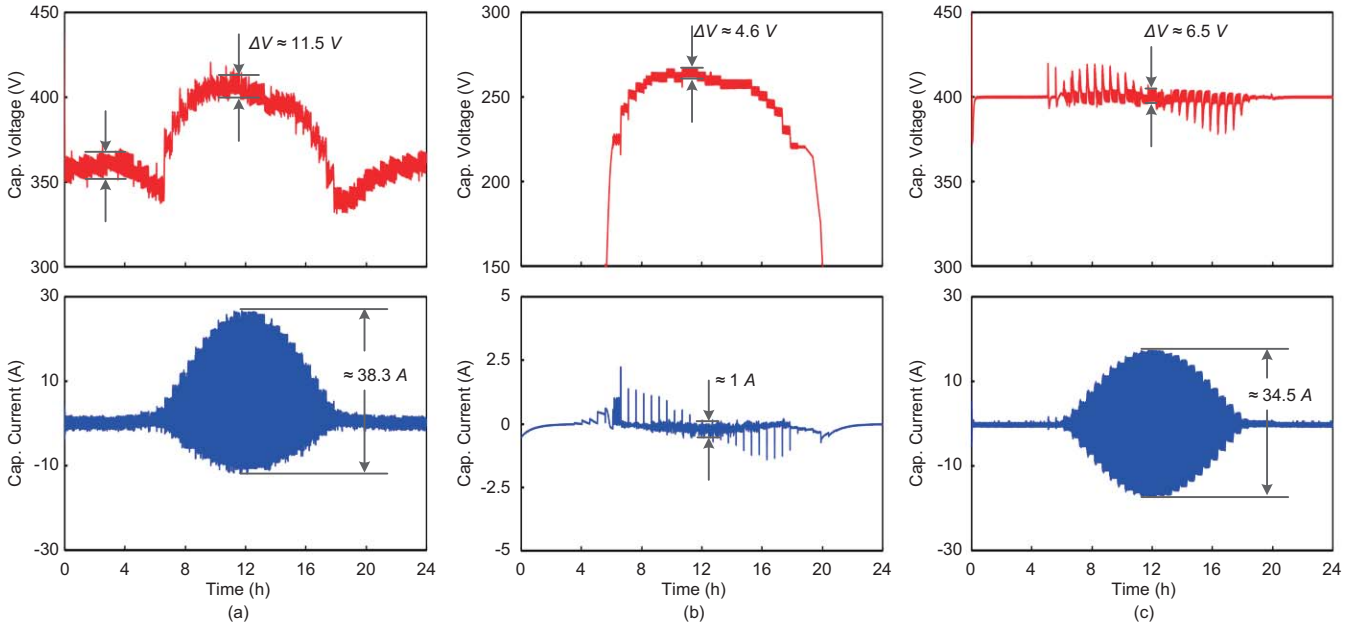

Fig. 6. Translated capacitor voltage and current stresses in single-phase grid connected PV systems under a daily real-field mission profile (30 min per sample) shown in Fig. 5: (a) stresses of the capacitor C_{dc1} in a single-stage PV system, (b) stresses of the PV-side capacitor C_{pv2} in a double-stage PV system, and (c) stresses of the inverter-side capacitor C_{dc2} in a double-stage system.

phase grid-connected PV systems. The nominal power of the PV panels is $P_{PV} \approx 3$ kW, and the power of each PV panel is 65 W under standard test conditions (ambient temperature: 25 °C, solar irradiance level: 1000 W/m^2), as shown in Table III. Consequently, in the case of a single-stage configuration, two PV strings are connected in parallel and each PV string consists of 23 PV panels in series, and the corresponding voltage at Maximum Power Point (MPP) is 406 V in the single-stage system under standard test conditions. For a double-stage system, three PV strings are in parallel and each PV string has 15 PV panels in series, and thus the voltage at MPP is 266 V, when the ambient temperature is 25 °C and the solar irradiance level is 1000 W/m^2. The control systems are presented in Fig. 2. A PR controller has been used as the current controller, and a second order generalized integrator PLL system has been adopted for synchronization [2]. The parameters of the controllers are listed in Table IV. A Perturb & Observe (P&O) MPPT algorithm is adopted [21], and an adaptive perturbing step-size $\Delta I_S = \frac{S}{S_n}\Delta I$ with S being the instantaneous solar irradiance level, $S_n = 1000$ W/m^2 being solar irradiance level under standard conditions, and $\Delta I = 0.1$ A in the double-stage system. While a fixed perturbing step-size ΔV of 2 V is adopted in the case of a single-stage configuration. The electrical stresses of the capacitors translated from the mission profile are shown in Fig. 6.

It can be observed in Fig. 6 that the capacitors at the terminals of PV panels (e.g. C_{dc1}) have experienced a wide range of voltage variations (330 V $\sim$ 415 V) through the day, because the PV-side capacitors are directly "exposed" to the mission profile and "modified" by the MPPT, when it is compared to the inverter-side capacitor C_{dc2} in a double-stage system. Besides, both the short-term steady-state voltage and current ripples of the PV-side capacitor C_{dc1} in a single-stage system (e.g. 11.5 V and 38.3 A) are also higher than the ripples of the inverter-side capacitor C_{dc2} in a double stage system (e.g. 6.5 V and 34.5 A) as shown in Fig. 6 (a) and (c), although the capacitance of the two capacitors is the same, i.e. $C_{dc1} = C_{dc2} = 1100$ μF. The results confirmed the above analysis, where it is implied that the capacitor in a single-

TABLE III
PARAMETERS OF A SOLAR PV PANEL (BP365).

Parameter	Symbol	Value	Unit
Rated power	P_{mpp}	65	W
Voltage at P_{mpp}	V_{mpp}	17.6	V
Current at P_{mpp}	I_{mpp}	3.69	A
Open circuit voltage	V_{OC}	21.7	V
Short circuit current	I_{SC}	3.99	A
Temp. coefficient of I_{SC}	-	0.065±0.015	%/°C
Temp. coefficient of V_{OC}	-	-(80±10)	mV/°C

TABLE IV
PARAMETERS OF THE CONTROLLERS SHOWN IN FIG. 2.

Parameter	Value
MPPT PI controller (single-stage)	$k_{p1} = 1.05$ - proportional gain $k_{i1} = 75$ - integrator gain
DC-link PI controller (double-stage)	$k_{p2} = 0.1$ - proportional gain $k_{i2} = 1.26$ - integrator gain
MPPT controller (double-stage)	$k_{mpp} = 1000$
Current controller (both systems)	$k_{pr} = 20$ - proportional gain $k_{ir} = 2000$ - resonant gain

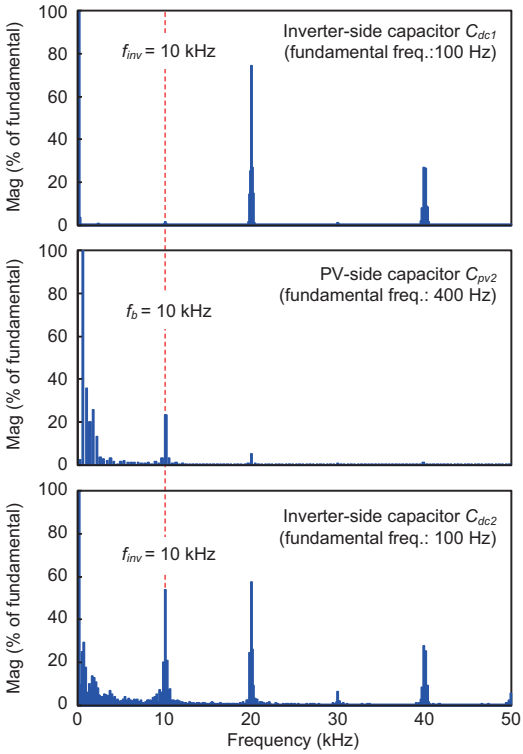

Fig. 7. Harmonic spectrums of the capacitor steady-state ripple currents in both systems shown in Fig. 1 under the standard test conditions (1000 W/m^2, 25 °C).

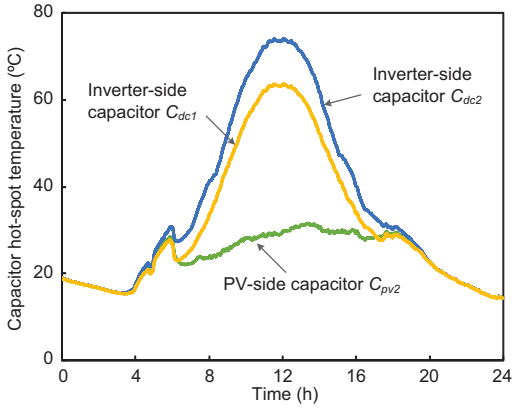

Fig. 8. Translated thermal stresses of the capacitors in the 1 kW single-phase PV systems under a daily mission profile (5 min per sample) shown in Fig. 5.

stage system is more stressful than the DC-link capacitor in a double-stage system, since the only capacitor C_{dc1} in a single-stage system has to decouple the double-grid frequency power variation and also the PV power of intermittency. Besides, the stresses of the PV-side capacitor C_{pv2} in a double-stage system are also mainly affected by the mission profile (e.g. the voltage stress: 225 V to 270 V from 6:00 am to 19:00 pm). As it has only to decouple the fluctuating power of high switching frequency components, the steady-state ripples of this capacitor are also smaller, which is in agreement with the above analysis.

Fig. 6 has also illustrated that these capacitors might be under high voltage/current transient ripples, which are induced by mission profiles. Notably, this study is carried on a clear daily mission profile shown in Fig. 5. In the case of a mission profile with running clouds, where the solar irradiance may present large step-changes, the capacitors at the PV-side (C_{dc1} and C_{pv2}) will experience more sudden variations. These transient ripples will affect the capacitor lifetime and may make the capacitors fail to operate suddenly. In contrast to those capacitors placed at the PV-side, although the transient ripples of the capacitor C_{dc2} at the inverter-side in a double-stage system are also induced by mission profiles, the ripples could be alleviated by tuning the inverter control parameters or by adding auxiliary power decoupling circuits [10], [11], [24]. In summary, from a design point of view, the capacitors at the PV side (C_{dc1} and C_{pv2}) should have the ability to handle a wide range of voltage variations due to mission profile effects, and the inverter control parameters should be tuned appropriately to reduce both voltage and current transient ripples of the capacitor at the inverter input (C_{dc2}). It has been demonstrated by the translated capacitor loading that the mission profiles have a significant impact on the capacitor electrical stresses/ripples.

According to (3), in order to further investigate the thermal performance of those capacitors, the ripple currents shown in Fig. 6 have to be decomposed using the FFT analysis to calculate the total power losses. The harmonic content of the capacitor ripple currents in steady-state under the standard test conditions is exemplified in Fig. 7, which shows that the switching frequency harmonics are not negligible. Due to this necessity of off-line FFT analysis for the power loss calculation, it is not possible to translate the mission profile to the thermal stress of the capacitors on-line. In this paper, a temperature look-up table of the capacitors has been adopted. The look-up table is created according to the off-line FFT analysis of the simulated ripple currents under different ambient conditions. It takes the mission profile as the input and outputs the thermal loading [25]. The mission profile shown in Fig. 5 is then directly translated to the capacitor thermal loading, as it is presented in Fig. 8. It can be seen in the translated thermal stresses that the PV-side capacitor (C_{pv2}) in a double-stage system has the lowest temperature loading. The inverter-side capacitors (C_{dc1} and C_{dc2}) are under much thermal loading, due to the high voltage stress and current ripples as shown in Fig. 6. It should be pointed out that the resultant thermal stresses shown in Fig. 8 are obtained only in consideration of a limited number of harmonic currents (e.g. currents of 100 Hz for C_{dc1} and C_{dc2}, current harmonic components of 400 Hz and 800 Hz for C_{pv2}). Thus, Fig. 8 only offers a qualitative comparison of the capacitor thermal performances. Quantitatively translated capacitor stresses can be enabled, when the major harmonic currents shown in Fig. 7 are taken into account. In that case, a more detailed look-up table can be built up, which will be a further in-depth study.

IV. Operating Condition Effects on Capacitors

The next-generation PV inverters have to be of much power controllability and flexibility in order to integrate into the conventional grid smoothly with reduced cost of PV energy [26], [27]. One of the advanced features for PV inverters is to statically support the grid by appropriately controlling the active power and exchanging the reactive power [4], and also to ride-through transient grid disturbances [27]–[29]. Thus, the future PV systems have to remain connected to the grid during low-voltage transients and also to support the grid voltage recovery by injecting reactive power into the grid.

In the case of low voltage ride-through operation, the DC-link capacitor stresses in the PV systems will be affected [13]. To further investigate the operation condition effects on the capacitor stresses in PV systems, a single-phase single-stage 1 kW PV system under grid faults is demonstrated by simulations and experiments, where the grid voltage has experienced a voltage sag of 0.45 p.u. (i.e. grid voltage $v_{g,RMS} = 126.5$ V during fault transients) in a period of 500 ms. Two capacitors are configured in parallel as the DC-link C_{dc1} of this system referring to Fig. 1(a), and the capacitor parameters are shown in Table II. The control parameters are the same as those in the previous study. The results are shown in Fig. 9 and Fig. 10.

During fault ride-through, the system is operating at low voltage ride through mode instead of MPPT mode at unity power factor, where the active power is reduced in order to inject sufficient reactive power for grid support and also prevent the inverter from over-current trip-off [26]. It can be observed in Fig. 9 and Fig. 10 that, with low voltage ride-through control, the current stress of the capacitor C_{dc1} is reduced, while the voltage stress on the capacitor is increased, compared to those in MPPT operation mode with maximized active power injection. This is because that the peak amplitude of the injected grid current i_g is maintained almost constant under this low grid voltage transient. Moreover, as it is shown in Fig. 9, the internal hot-spot temperature of the capacitor due to the power losses induced by ripple currents according to (4) is also reduced under grid faults when the low voltage ride-through control is enabled. Since the operating hours of the capacitors are mainly dependent on the internal hot-spot temperature [13], [15], improvement of the capacitor lifetime is then achieved by the low voltage ride-through control.

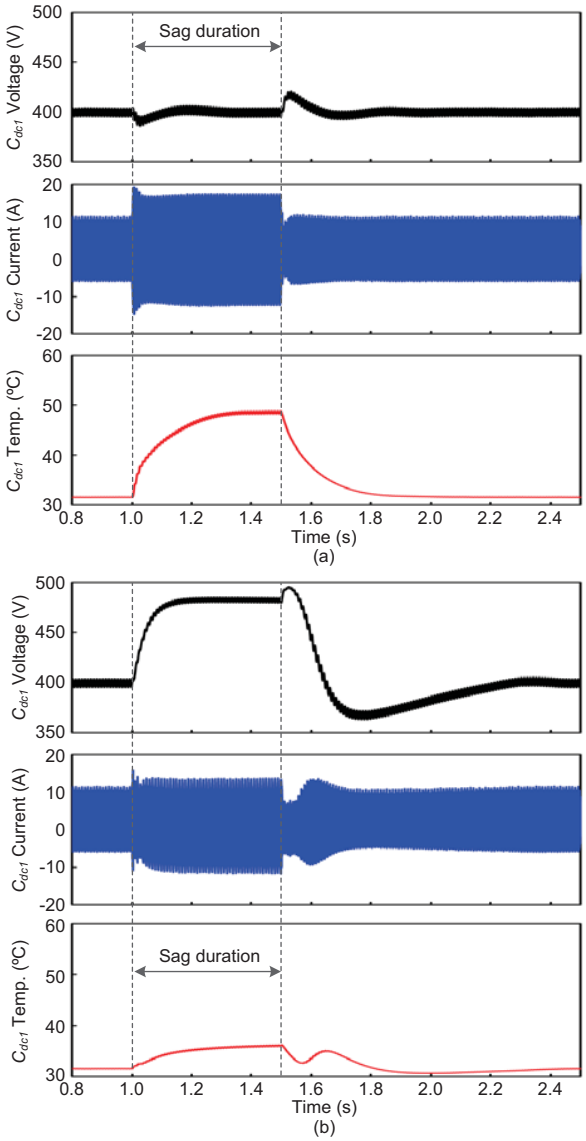

Fig. 9. Stresses of the capacitor (C_{dc1}) in a 1 kW single-phase PV system shown in Fig. 1(a) under a grid fault (top: capacitor voltage, middle: capacitor current, bottom: capacitor temperature, voltage sag level: 0.45 p.u.): (a) without and (b) with low voltage ride through control (active power: 0.37 p.u. and reactive power: 0.5 p.u.).

V. Conclusion

In this paper, the stresses (both electrical and thermal loading) on the capacitors in single-phase grid-connected PV systems have been translated from a real-field daily mission profile and the fault ride-through operation. According to the simulation results of both single-stage and double-stage PV systems, and the experiments on a double-stage PV system, it can be concluded that the mission profile has a significant impact on the stresses of DC-link capacitors, especially the capacitors connected at the terminal of the PV panels. Moreover, under grid faults, the capacitor current stress is reduced with low voltage ride-through control, leading to a lower temperature stress on the capacitor. However, the voltage stress is increased since the active power production of the PV panels is reduced in order to inject sufficient reactive power during fault ride-through. Those results have implied that the design of DC-link capacitors should take the effects from both mission profiles and system operation conditions into account, and many trade-offs, which have not yet been considered in the past, have to be considered in the future. It is suggested that the design of reliable capacitor in power electronics based systems (e.g. PV systems) has to include one more stringent consideration - thermal performance in addition to voltage ripple, current ripple, maximum voltage during transient (e.g. voltage faults), system stability, and etc..

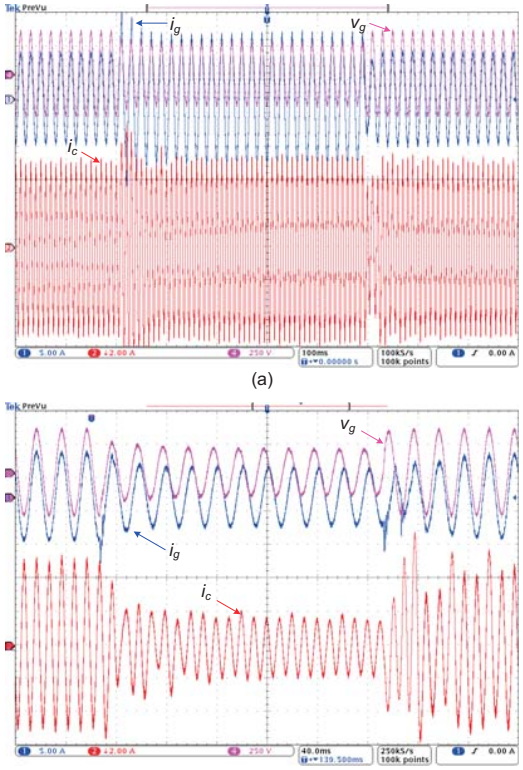

Fig. 10. Experimental results of a 1 kW single-phase single-stage PV system shown in Fig. 1(a) under a grid fault (0.45 p.u. voltage sag): grid voltage v_g [250 V/div], grid current i_g [5 A/div], capacitor fundamental (100 Hz) current i_c [2 A/div] under a grid fault: (a) without low voltage ride through (time: 100 ms/div) and (b) with low voltage ride through control (time: 40 ms/div, active power: 0.3 p.u. and reactive power: 0.49 p.u.).

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